LISTING OF THE CLAIMS

1. (Original) A software representation of a plurality of programmable hardware tiles included in a programmable logic device (PLD), each hardware tile including common routing resources common to all of the hardware tiles and unique logic resources unique to each hardware tile, the software representation comprising:

a common software tile comprising a description of the common routing resources, the common software tile having first terminals for coupling an instance of the common software tile to other instances of the common software tile and further having second terminals; and

for each hardware tile, a unique software tile comprising a description of the unique logic resources included in the hardware tile, each unique software tile comprising terminals for coupling the unique software tile to the second terminals of an instance of the common software tile.

2. (Original) The software representation of Claim 1, wherein:

each hardware tile further includes unique routing resources unique to each hardware tile; and

the unique software tile for each hardware tile further comprises a unique description of the unique routing resources included in the hardware tile.

3. (Original) The software representation of Claim 1, wherein the PLD is a Field Programmable Gate Array (FPGA).

4. (Original) The software representation of Claim 3, wherein the plurality of programmable hardware tiles comprises at least one of the following types of logic blocks: configurable logic blocks (CLBs), Random Access Memory (RAM) blocks, multiplier blocks, and processor blocks.

5. (Original) The software representation of Claim 4, wherein the plurality of programmable hardware tiles further comprises input/output blocks (IOBs).

6. (Original) The software representation of Claim 1, further comprising a PLD device model representing a placement of the plurality of programmable hardware tiles in the PLD and comprising instances of the common software tile and the unique software tiles, the PLD device model utilizing a uniform numbering scheme based on numbered instances of the common software tile.

7. (Original) The software representation of Claim 1, wherein the plurality of programmable hardware tiles comprises an entirety of the programmable hardware tiles in the PLD.

8. (Original) A method of representing a plurality of programmable hardware tiles included in a programmable logic device (PLD), each hardware tile including common routing resources common to all of the hardware tiles and unique logic resources unique to each hardware tile, the method comprising:

generating a common software tile comprising a description of the common routing resources, the common software tile having first terminals for coupling an instance of the common software tile to other instances of the common software tile and further having second terminals; and

generating, for each hardware tile, a unique software tile comprising a description of the unique logic resources included in the hardware tile, each unique software tile comprising terminals for coupling the unique software tile to the second terminals of an instance of the common software tile.

9. (Original) The method of Claim 8, wherein:

each hardware tile further includes unique routing resources unique to each hardware tile; and

generating the unique software tile for each hardware tile further comprises generating a unique description of the unique routing resources included in the hardware tile.

10. (Original) The method of Claim 8, wherein the PLD is a Field Programmable Gate Array (FPGA).

11. (Original) The method of Claim 10, wherein the plurality of programmable hardware tiles comprises at least one of the following types of logic blocks: configurable logic blocks (CLBs), Random Access Memory (RAM) blocks, multiplier blocks, and processor blocks.

12. (Original) The method of Claim 11, wherein the plurality of programmable hardware tiles further comprises input/output blocks (IOBs).

13. (Original) The method of Claim 8, further comprising generating a PLD device model representing a placement of the plurality of programmable hardware tiles in the PLD and comprising instances of the common software tile and the unique software tiles, the PLD device model utilizing a uniform numbering scheme based on numbered instances of the common software tile.

14. (Original) The method of Claim 8, wherein the plurality of programmable hardware tiles comprises an entirety of the programmable hardware tiles in the PLD.

15. (Original) A computer-readable storage medium comprising a software representation of a plurality of programmable hardware tiles included in a programmable logic device (PLD), each hardware tile including common routing resources common to all of the hardware tiles and unique logic resources unique to each hardware tile, the medium comprising:

a common software tile comprising a description of the common routing resources, the common software tile having first terminals for coupling an instance of the common software tile to other instances of the common software tile and further having second terminals; and

for each of the plurality of programmable hardware tiles, a unique software tile comprising a description of the unique logic resources included in the hardware tile, each unique software tile comprising terminals for coupling the unique software tile to the second terminals of an instance of the common software tile.

16. (Original) The computer-readable storage medium of Claim 15, wherein:

each hardware tile further includes unique routing resources unique to each tile; and

the unique software tile for each hardware tile further comprises a unique description of the unique routing resources included in the hardware tile.

17. (Original) The computer-readable storage medium of Claim 15, wherein the PLD is a Field Programmable Gate Array (FPGA).

18. (Original) The computer-readable storage medium of Claim 17, wherein the plurality of programmable hardware tiles comprises at least one of the following types of logic blocks: configurable logic blocks (CLBs), Random Access Memory (RAM) blocks, multiplier blocks, and processor blocks.

19. (Original) The computer-readable storage medium of Claim 18, wherein the plurality of programmable hardware tiles further comprises input/output blocks (IOBs).

20. (Original) The computer-readable storage medium of Claim 15, further comprising a PLD device model representing a placement of the plurality of programmable hardware tiles in the PLD and comprising instances of the common software tile and the unique software tiles, the PLD device model utilizing a uniform numbering scheme based on numbered instances of the common software tile.

21. (Original) The computer-readable storage medium of Claim 15, wherein the plurality of programmable hardware tiles comprises an entirety of the programmable hardware tiles in the PLD.